524,288K WORD x 8 Bit High Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 70,85,100ns(Max.)**
- **Low Power Dissipation**
  Standby (CMOS) : 11mW(Typ.)
  1.1μW(Typ.) L-Version
  275μW(Typ.) LL-Version
  Operating : 137.5mW(Max.)
- **Single 5V±10% power supply**
- **Wide temperature operatint: -40°C~85°C**
- **TTL Compatible inputs and outputs**
- **Three State Output**
- **Low Data Retention Voltage:2V(Min)**
- **Standard Pin Configuration**
  KM684000LGI/LGI-L : 32-SOP-525
  KM684000LTI/LTI-L : 32-TSOP2-400F
  KM684000LRI/LRI-L : 32-TSOP2-400R

GENERAL DESCRIPTION

The KM684000LI/LI-L is a 4,194,304-bit high-speed Static Random Access Memory organized as 524, 288 words by 8 bits.
The device is fabricated using Samsung's advanced CMOS process.
The KM684000LI/LI-L has an output enable input for precise control of the data outputs.
It also has chip enable inputs for the minimum current power down mode
The KM684000LI/LI-L has been designed for high speed and low power applications.
It is particularly well suited for battery back-up nonvolatile memory application.

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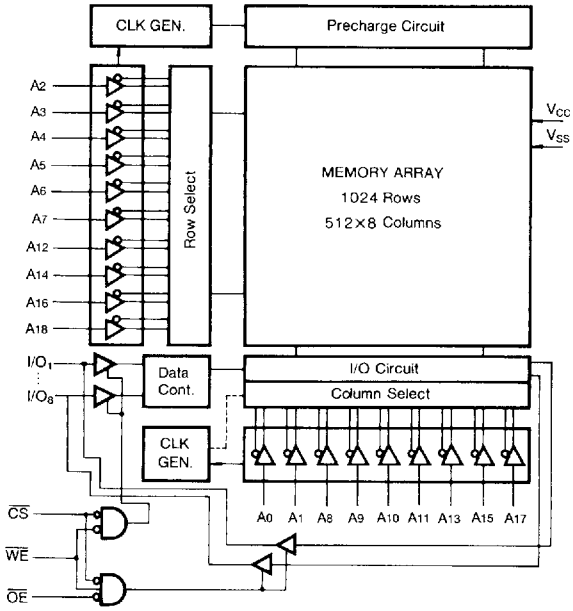
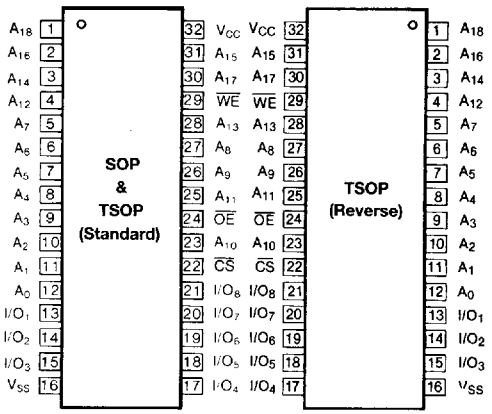
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A18	Address Inputs
$\overline{WE}$	Write Enable input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable input
I/O1~I/O8	Data Inputs/Outputs
VCC	Power(+5V)
VSS	Ground

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ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

* Stresses greater than those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=40 to 85°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.3*	—	0.8	V

* V_{IL}(min.)=-3.0V for < 50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=-40 to 85°C, V_{CC}=5V±10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-1	+1	μA
Output Leakage Current	I_{IO}	$\overline{CS}$=V_{IN} or $\overline{WE}$=V_{IL} $\overline{OE}$=V_{IH}, $V_{I/O}$=Vss to V_{CC}		-1	+1	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, $I_{I/O}$=0mA			25	mA
Average Operating Current	I_{CC1}	Cycle Time=1μs, 100% Duty $\overline{CS}$≤0.2V, V_{IH}≥V_{CC}-0.2V V_{IL}≤ 0.2V, $I_{I/O}$=0mA			20	mA
	I_{CC2}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL} V_{IN}=V_{IL} or V_{IH} I_{IO}=0mA			70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}			3	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V	L		100	μA
		V_{IN}≥V_{CC}-0.2 or V_{IN}≤0.2V	L-L		50	μA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1.0mA		2.4		V

CAPACITANCE (f=1MHz, T_A=25°C)

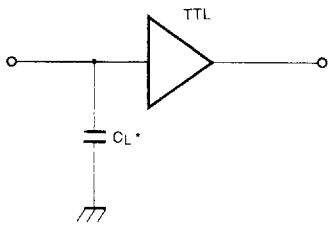
Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	10	pF

* Note : Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=-40 to 85°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	C_L=100pF+1TTL

TEST CIRCUIT



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	KM684000LI-7 KM684000LI-7L		KM684000LI-8 KM684000LI-8L		KM684000LI-10 KM684000LI-10L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		ns
Address Access Time	t_{AA}		70		85		100	ns
Chip Select to Output	t_{CO}		70		85		100	ns
Output Enable to Valid Output	t_{OE}		35		40		50	ns
Chip Enable to Low-Z Output	t_{LZ}	10		10		10		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		5		ns
Output Disable to High-Z Output	t_{HZ}	0	25	0	30	0	30	ns
Output Disable to High-Z Output	t_{OHZ}	0	25	0	30	0	30	ns
Output Hold from Address Change	t_{OH}	10		10		10		ns

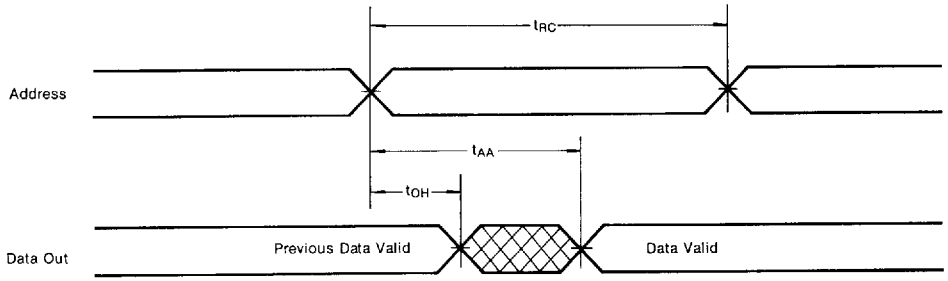
WRITE CYCLE

Parameter	Symbol	KM684000LI-7 KM684000LI-7L		KM684000LI-8 KM684000LI-8L		KM684000LI-10 KM684000LI-10L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		ns
Chip Select to End of Write	t_{CW}	60		70		80		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	60		70		80		ns
Write Pulse Width	t_{WP}	50		55		60		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	30	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	30		35		40		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		5		ns

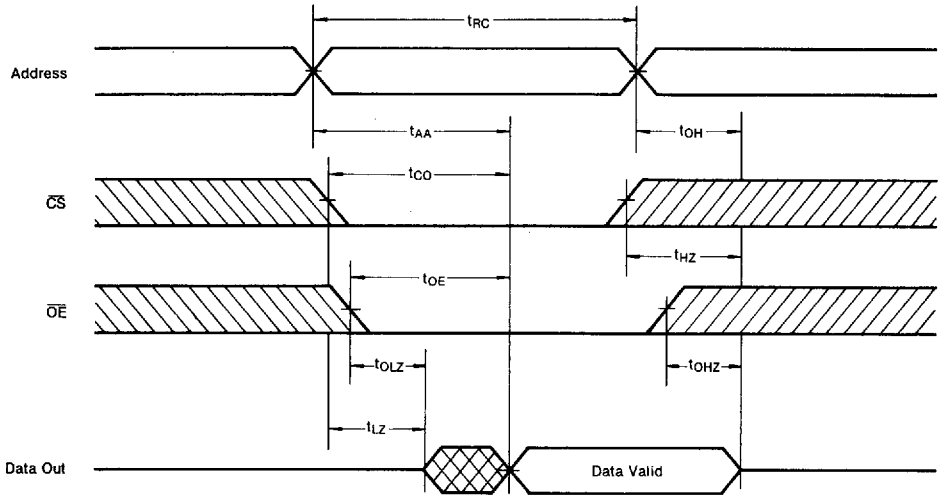
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

($\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



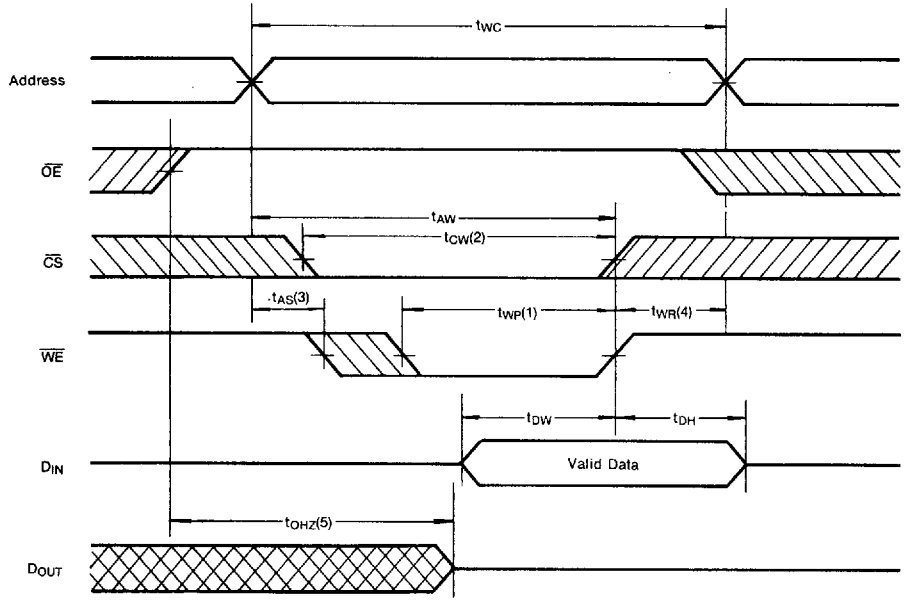
TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ = Clock)



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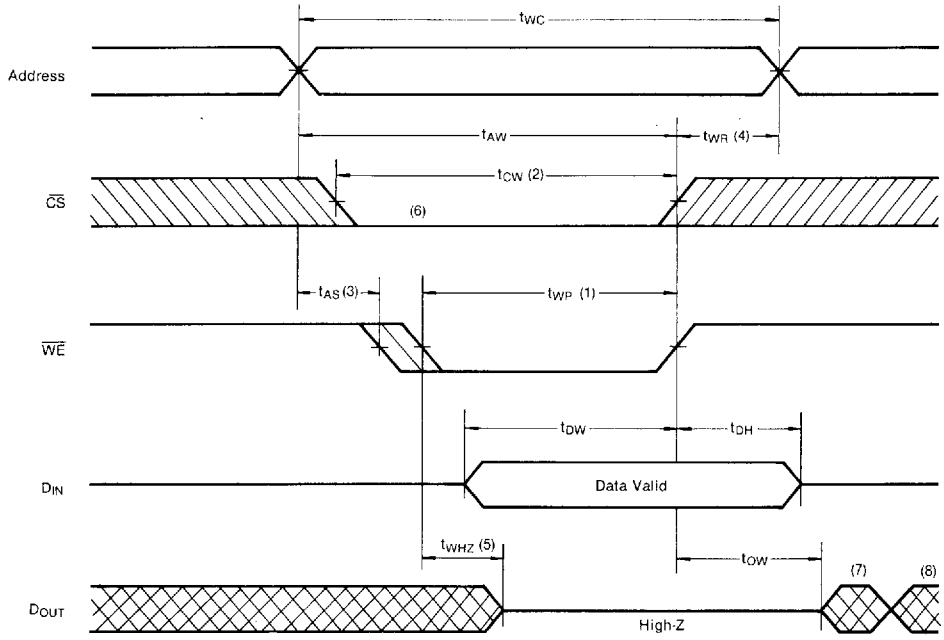
TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ = Low Fixed)



Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earlist transition among $\overline{CS}$ going high and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or WE going high.
5. During this period, the I/O pins are in the outputs Low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
7. D_{OUT} is the some phase of latest written data in this write cycle.
8. D_{OUT} is the read data of the new address.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current
H	X*	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS* (T_A=40 to 85°C)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
V_{CC} for Data Retention	V_{dr}	$\overline{CS} \geq V_{CC}$-0.2V		2.0		5.5	V
Data Retention Current	I_{dr}	V_{CC}=3V	L			50*	μA
		$\overline{CS} \geq V_{CC}$-0.2V	L-L			20**	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention Wave forms (below)		0			ns
Recovery Time	t_{RDR}			5			ns

* 20μA (max) at 0°C~40C°
** 5μA (max) at 0°C~40C°

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DATA RETENTION WAVEFORM

L/L-L Power Version